Filtronic

FPD3000SOT89

Datasheet v3.0

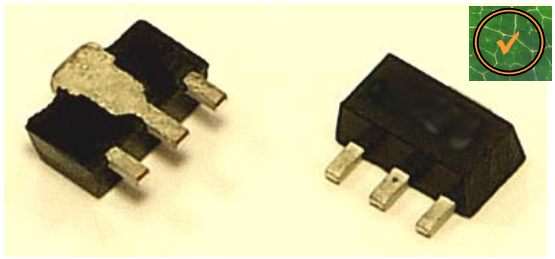
LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1850MHZ):

- 30 dBm Output Power (P1dB)
- 13 dB Small-Signal Gain (SSG)
- 1.3 dB Noise Figure
- 45 dBm Output IP3
- 45% Power-Added Efficiency
- FPD3000SOT89E: RoHS compliant (Directive 2002/95/EC)

PACKAGE:

RoHS



GENERAL DESCRIPTION:

The FPD3000SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 3000 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The double recessed Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and i/p power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	29	30		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	11.5	13		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		45		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS VDS = 5 V; IDS = 25% IDSS		1.3 0.9		dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3		 42 45		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	750	930	1100	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		1.5		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		800		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		2	20	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 3 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 3 mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 3 mA	12	16		V
Thermal Resistance	RθJC			35		°C/W

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f = 1850 MHz using CW signal (except as noted)

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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < -0.5V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDss
Gate Current	IG	Forward or reverse current	30mA
RF Input Power[2]	PIN	Under any acceptable bias state	600mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-40°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	3.5W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

Notes:

[1] $T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device

[2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1

[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

[4] Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,

where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power

Total Power Dissipation to be de-rated as follows above 22°C:

P_{TOT}= 3.5 - (0.028W/°C) x T_{PACK}

where T_{PACK}= source tab lead temperature above 22°C

(coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 65°C carrier temperature: P_{TOT} = 3.5W – (0.028 x (65 – 22)) = 2.3W

BIASING GUIDELINES:

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A Class A/B Bias of 25% to 33% of IDSS to achieve better OIP3 performance is suggested.

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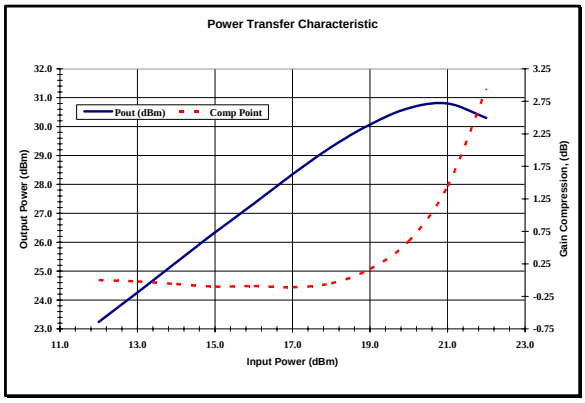
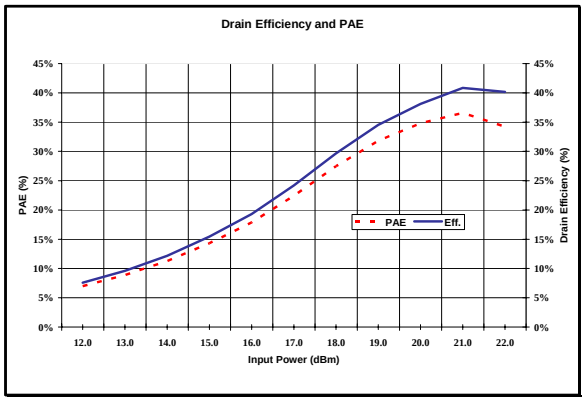
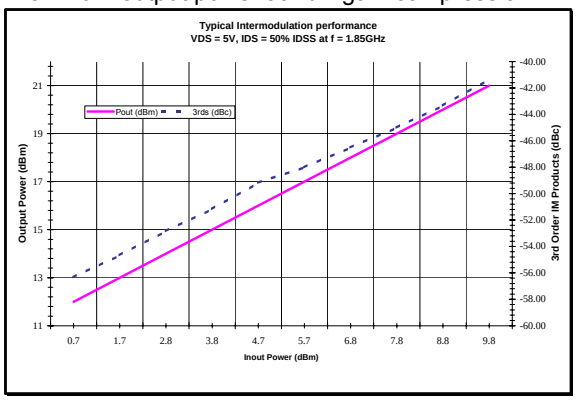
TYPICAL TUNED RF PERFORMANCE:

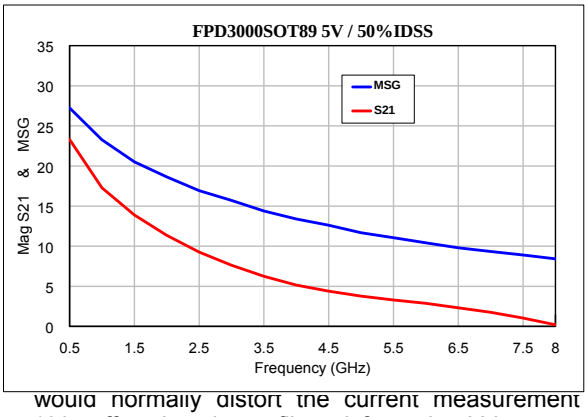




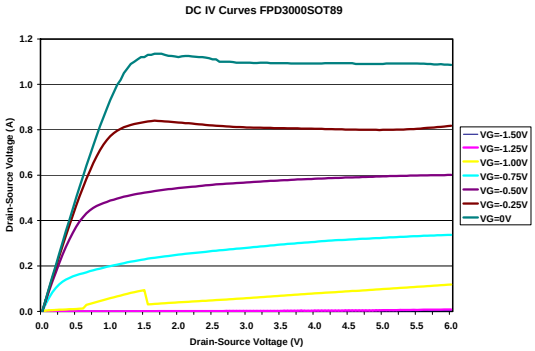
NOTE: Typical power and efficiency is shown above. The devices were biased nominally at V_{DS} = 5V, I_{DS} = 50% of I_{DSS}, at a test frequency of 1.85 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.



Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P1dB + 14 dB. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.



TYPICAL I-V CHARACTERISTICS:



would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

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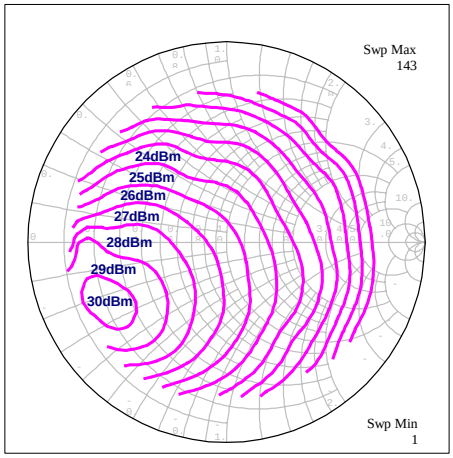
TYPICAL OUTPUT PLANE POWER CONTOURS: (VDS = 5v, IDS = 50%IDSS)



1850 MHz

Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

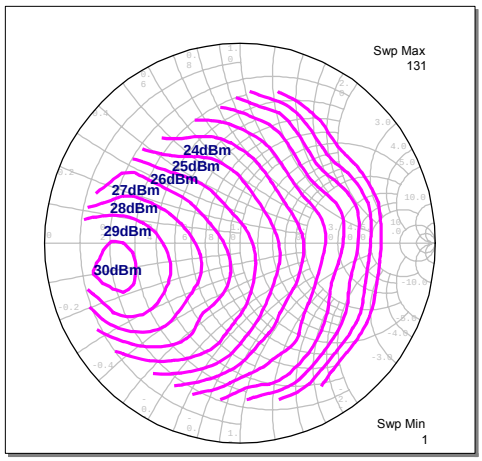
Input (Source plane) Γ_s:

0.70 ∠ -165.5º

0.17 - j0.12 (normalized)

8.5 – j6.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.



900 MHz

Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

Input (Source plane) Γ_s:

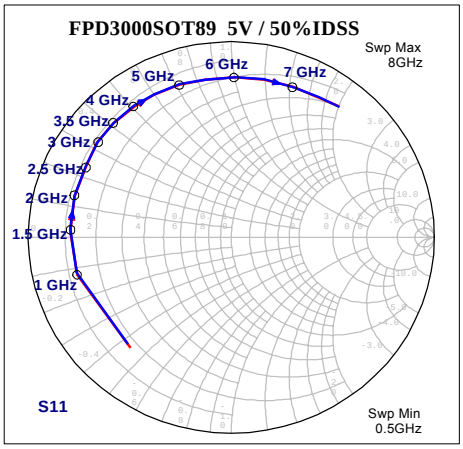
0.78 ∠ -147.4º

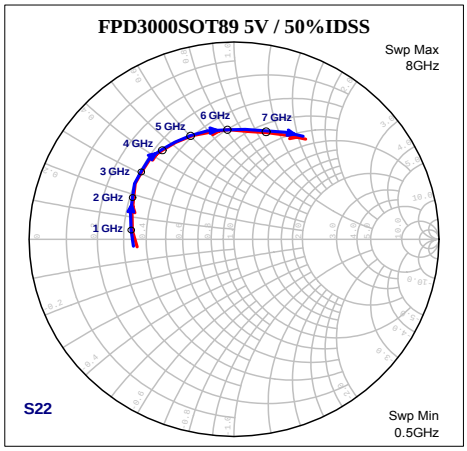
0.13 - j0.29 (normalized)

6.5 – j14.5 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM):





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S-PARAMETERS: (BIASED @ 5V, 50%IDSS)

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.050	0.946	-24.3	36.120	159.0	0.006	79.8	0.175	-145.5
0.300	0.824	-97.5	19.282	120.3	0.027	56.8	0.384	-150.1
0.550	0.761	-132.1	12.243	103.2	0.037	45.6	0.478	-165.4
0.800	0.779	-150.7	8.992	91.8	0.043	40.5	0.507	-172.3
1.050	0.771	-163.6	7.020	84.0	0.048	38.3	0.522	-179.1
1.300	0.775	-173.0	5.802	76.3	0.054	35.9	0.529	176.4
1.550	0.779	178.6	4.934	70.1	0.059	34.7	0.528	171.9
1.800	0.775	171.1	4.306	63.6	0.064	31.7	0.532	167.4
2.050	0.778	164.5	3.834	57.8	0.069	29.8	0.529	163.2
2.300	0.780	158.1	3.444	52.0	0.074	27.5	0.531	158.7
2.550	0.777	152.3	3.131	46.1	0.080	24.3	0.531	154.2
2.800	0.778	146.8	2.878	40.4	0.085	22.1	0.534	149.1
3.050	0.782	142.6	2.636	34.9	0.088	19.1	0.537	143.6
3.300	0.784	137.7	2.459	29.4	0.093	15.6	0.544	138.2
3.550	0.785	133.2	2.286	24.0	0.097	12.7	0.545	132.9
3.800	0.790	129.0	2.146	18.7	0.101	9.6	0.551	127.8
4.050	0.790	124.8	2.017	13.3	0.105	5.7	0.555	123.2
4.300	0.806	120.7	1.896	9.0	0.106	4.5	0.575	118.8
4.550	0.800	115.1	1.821	3.4	0.113	1.5	0.574	113.3
4.800	0.794	111.6	1.728	-1.4	0.117	-2.0	0.575	109.7
5.050	0.800	107.0	1.648	-6.7	0.121	-5.4	0.577	105.9
5.300	0.801	102.6	1.576	-11.5	0.123	-8.6	0.580	102.6
5.550	0.805	98.0	1.516	-16.5	0.128	-11.8	0.583	98.7
5.800	0.806	93.8	1.461	-21.4	0.132	-14.7	0.583	95.2
6.050	0.808	89.5	1.411	-26.2	0.136	-18.0	0.586	91.1
6.300	0.810	85.4	1.360	-31.2	0.139	-21.3	0.588	86.9
6.550	0.811	81.3	1.317	-36.3	0.143	-24.6	0.593	82.4
6.800	0.814	77.4	1.272	-41.2	0.146	-28.2	0.592	77.7
7.050	0.818	73.2	1.232	-46.3	0.151	-31.7	0.601	73.0
7.300	0.821	69.0	1.189	-51.3	0.153	-35.1	0.607	68.2
7.550	0.829	64.8	1.149	-56.4	0.157	-38.8	0.614	63.5
7.800	0.831	60.2	1.108	-61.4	0.159	-42.5	0.623	59.3
8.050	0.839	55.5	1.066	-66.3	0.160	-46.5	0.634	55.3

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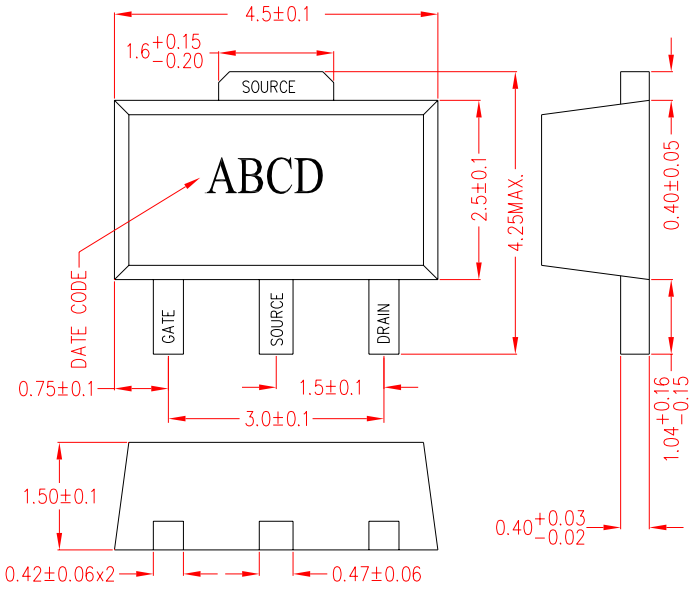
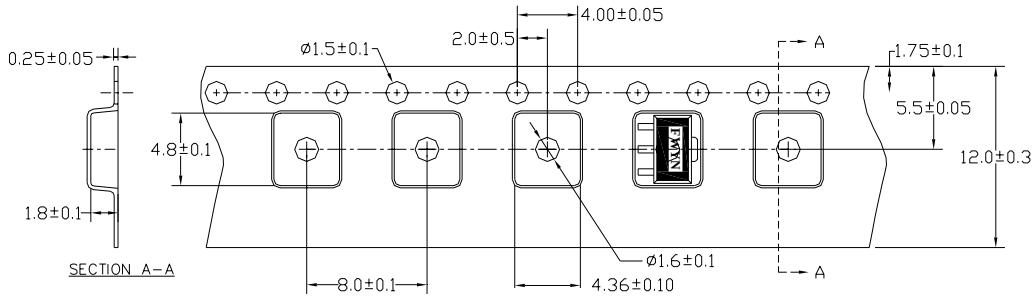
PACKAGE OUTLINE:

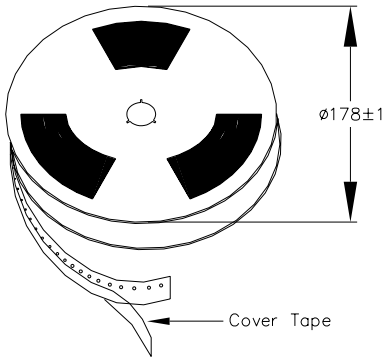
(dimensions in millimeters – mm)



TAPE DIMENSIONS AND PART ORIENTATION



DIMENSIONS ARE IN MM



- Also available with horizontal part orientation
- Hub diameter = 80mm
- Devices per reel = 1000

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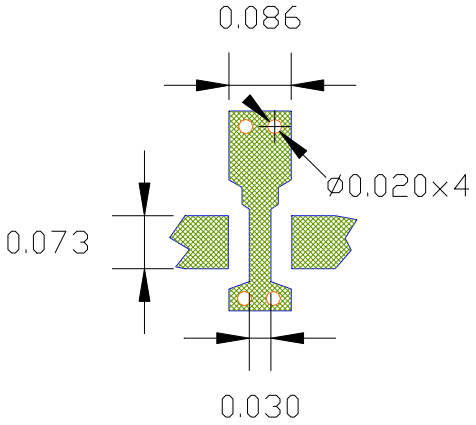
Device Foot Print:



Units in inches

Preferred Assembly Instructions:

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260°C.

Handling Precautions:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL Rating:

These devices should be treated as Class 0 (0-250 V) using the human body model as defined in JEDEC Standard No. 22-A114.

The device has a MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per, the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture / Reflow sensitivity classification for non-hermatic solid state surface mount devices.

Application Notes & Design Data:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

Reliability:

A MTTF of 4.2 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

Disclaimers:

This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information:

Part Number	Description
FPD3000SOT89	Packaged pHEMT
FPD3000SOT89E	RoHS compliant Packaged pHEMT
FPD3000SOT89(E)-BB	0.9 GHz evaluation board
FPD3000SOT89(E)-BA	1.85 GHz evaluation board
FPD3000SOT89(E)-BC	2.0 GHz evaluation board
FPD3000SOT89(E)-BD	2.2 GHz evaluation board
FPD3000SOT89(E)-BE	2.4 GHz evaluation board
FPD3000SOT89(E)-BG	2.6 GHz evaluation board

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